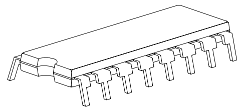
8-bit Constant Current LED Sink Driver

Features

- 8 constant-current output channels
- Constant output current invariant to load voltage change
- Excellent output current accuracy:
  between channels: < ±3% (max.), and
  between ICs: < ±6% (max.)
- Output current adjusted through an external resistor
- Constant output current range: 5 -120 mA
- Fast response of output current,
  $\overline{OE}$ (min.): 200 ns @I_{out} < 60mA
  $\overline{OE}$ (min.): 400 ns @I_{out} = 60~100mA
- 25MHz clock frequency
- Schmitt trigger input
- 3.3V~ 5V supply voltage
- Optional for "Pb-free & Green" Package

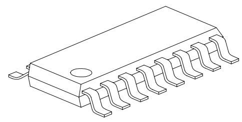
Current Accuracy		Conditions
Between Channels	Between ICs	
< ±3%	< ±6%	I_{OUT} = 10 ~ 100 mA, V_{DS} = 0.8V, V_{DD}= 5.0V

Dual In-Line Package



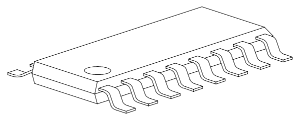
P-DIP16-300-2.54 Weight : 1.02g

Small Outline Package



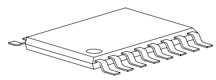
SOP16-150-1.27 Weight : 0.13g

Wide-body SOP



SOP16-300-1.27 Weight : 0.37g

Shrink SOP



SSOP16-150-0.64 Weight : 0.07g

Product Description

MBI5168 is designed for LED display applications. As an enhancement of its predecessor, MBI5001, MBI5168 exploits PrecisionDrive™ technology to enhance its output characteristics. MBI5168 contains a serial buffer and data latches, which convert serial input data into parallel output format. At MBI5168 output stage, eight regulated current ports are designed to provide uniform and constant current sinks for driving LEDs within a large range of Vf variations.

MBI5168 provides users with great flexibility and device performance while using MBI5168 in their system design for LED display applications, e.g. LED panels. Users may adjust the output current from 5 mA to 120 mA through an external resistor R_{ext}, which gives users flexibility in controlling the light intensity of LEDs. MBI5168 guarantees to endure maximum 17V at the output ports. The high clock frequency up to 25 MHz also satisfies the system requirements of high volume data transmission.

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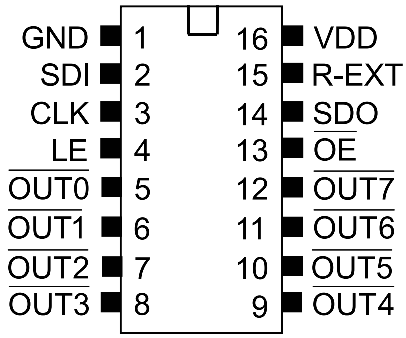
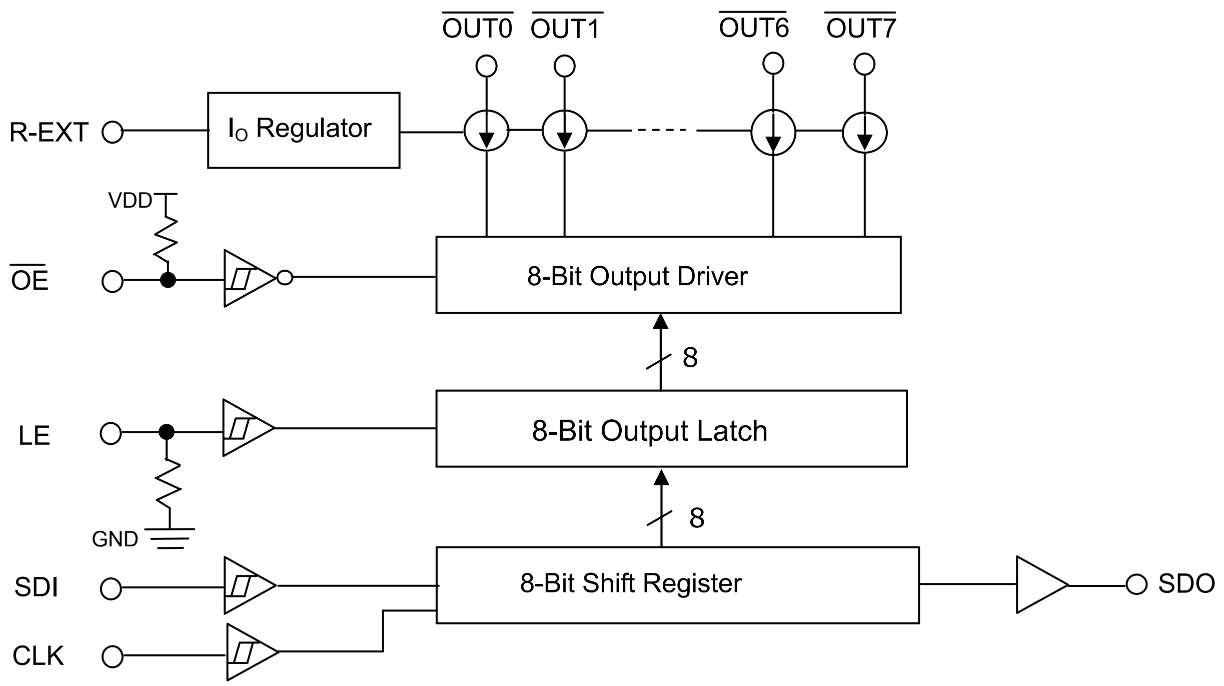
Terminal Description

Pin No.	Pin Name	Function
1	GND	Ground terminal for control logic and current sinks
2	SDI	Serial-data input to the shift register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low.
5-12	$\overline{\text{OUT0}}$ ~ $\overline{\text{OUT7}}$	Constant current output terminals
13	$\overline{\text{OE}}$	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
14	SDO	Serial-data output to the following SDI of next driver IC
15	R-EXT	Input terminal used to connect an external resistor for setting up output current for all output channels
16	VDD	Supply voltage terminal

Pin Description

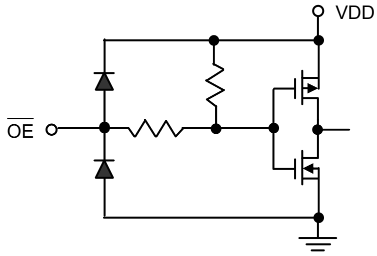


Block Diagram

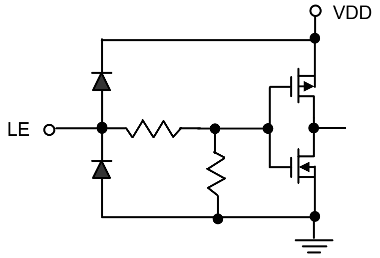


Equivalent Circuits of Inputs and Outputs

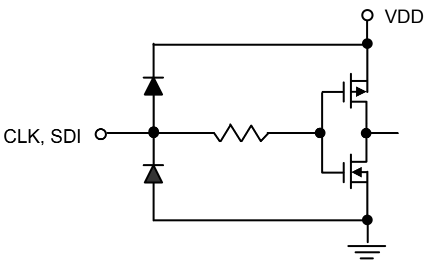
$\overline{OE}$ terminal



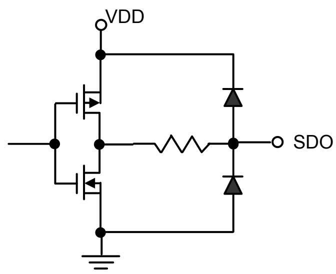
LE terminal



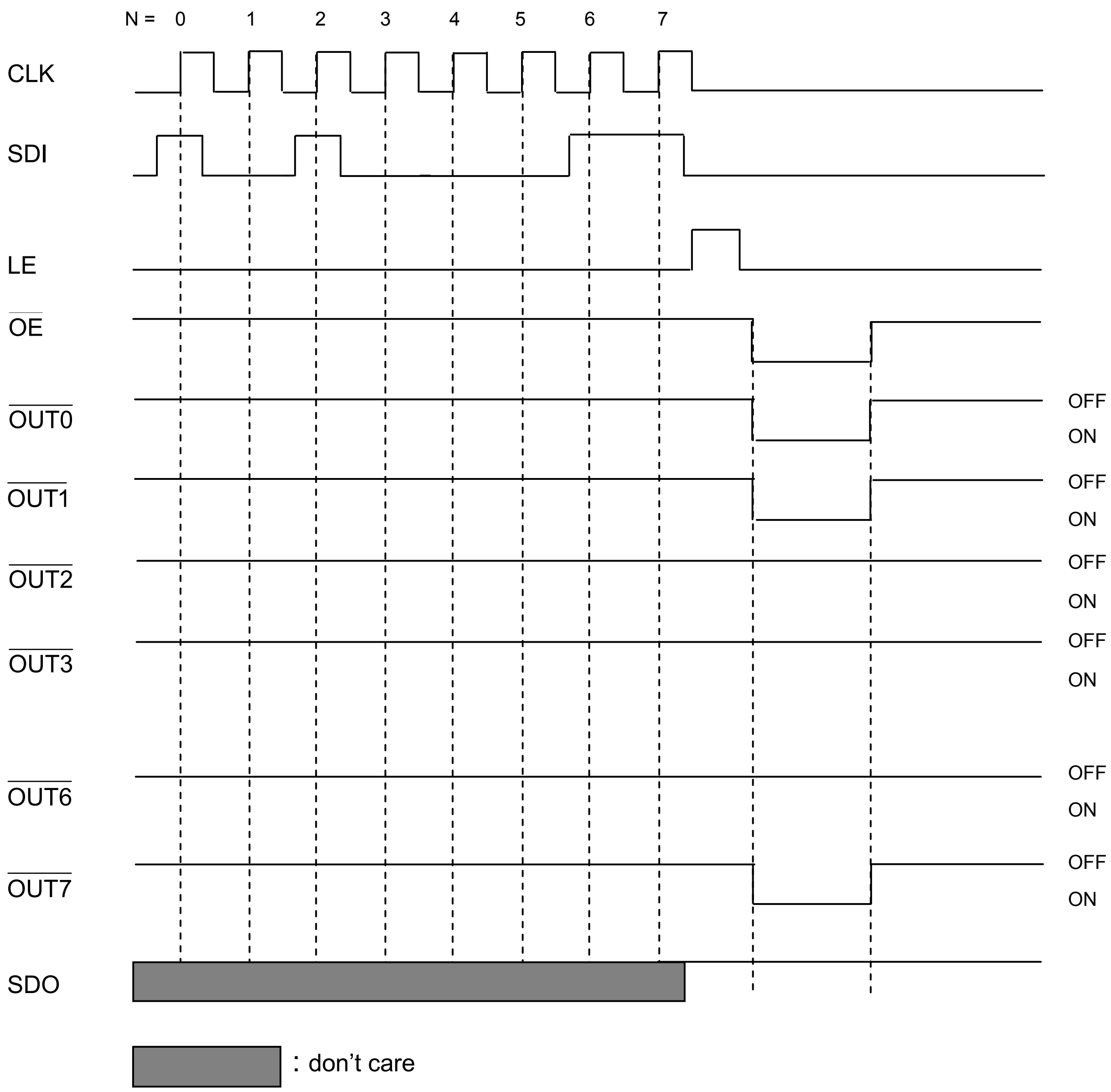
CLK, SDI terminal



SDO terminal



Timing Diagram



Truth Table

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$ … $\overline{OUT5}$ … $\overline{OUT7}$	SDO
↑	H	L	D_n	$\overline{D_n}$ ….. $\overline{D_{n-5}}$ …. $\overline{D_{n-7}}$	D_{n-7}
↑	L	L	D_{n+1}	No Change	D_{n-6}
↑	H	L	D_{n+2}	$\overline{D_{n+2}}$ …. $\overline{D_{n-3}}$ …. $\overline{D_{n-5}}$	D_{n-5}
↓	X	L	D_{n+3}	$\overline{D_{n+2}}$ …. $\overline{D_{n-3}}$ …. $\overline{D_{n-5}}$	D_{n-5}
↓	X	H	D_{n+3}	Off	D_{n-5}

Maximum Ratings

Characteristic			Symbol	Rating		Unit
Supply Voltage			V_{DD}	0 ~ 7.0		V
Input Voltage			V_{IN}	-0.4 ~ V_{DD}+0.4		V
Output Current			I_{OUT}	+120		mA
Output Voltage			V_{DS}	-0.5 ~ +20.0		V
Clock Frequency			F_{CLK}	25		MHz
GND Terminal Current			I_{GND}	1000		mA
Power Dissipation (On PCB, Ta=25°C)	CN	GN	P_D	1.55	1.66	W
	CD	GD		1.17	1.43	
	CDW	GDW		1.62	1.46	
	CP	GP		1.05	1.25	
Thermal Resistance (On PCB, Ta=25°C)	CN	GN	$R_{th(j-a)}$	64.35	60.20	°C/W
	CD	GD		85.82	70.14	
	CDW	GDW		61.63	68.67	
	CP	GP		94.91	80.00	
Operating Temperature			T_{opr}	-40 ~ +85		°C
Storage Temperature			T_{stg}	-55 ~ +150		°C

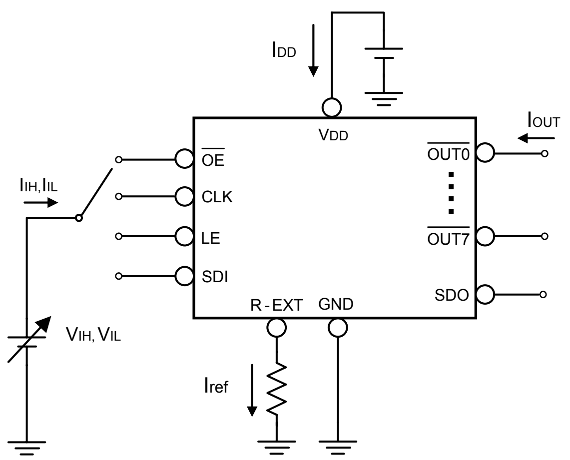
Electrical Characteristics (V_{DD}= 5.0V)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		4.5	5.0	5.5	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT7}$		-	-	17.0	V
Output Current		I_{OUT}	Test Circuit for Electrical Characteristics		5	-	120	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC		$0.7V_{DD}$	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC		GND	-	$0.3V_{DD}$	V
Output Leakage Current			V_{OH} = 17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} = +1.0mA		-	-	0.4	V
		V_{OH}	I_{OH} = -1.0mA		4.6	-	-	V
Output Current 1		I_{OUT1}	V_{DS} = 0.5V	R_{ext} = 744 Ω	-	25.26	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OUT} = 25.26mA $V_{DS} \geq$ 0.5V	R_{ext} = 744 Ω	-	±1	±3	%
Output Current 2		I_{OUT2}	V_{DS} = 0.6V	R_{ext} = 372 Ω	-	50.52	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OUT} = 50.52mA $V_{DS} \geq$ 0.6V	R_{ext} = 372 Ω	-	±1	±3	%
Output Current 3		I_{OUT3}	V_{DS} = 0.8V	R_{ext} = 186 Ω	-	101.0	-	mA
Current Skew (between channels)		dI_{OUT3}	I_{OUT} = 101.0mA $V_{DS} \geq$ 0.8V	R_{ext} = 186 Ω	-	±1	±3	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V		-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 4.5V and 5.5V		-	±1	-	% / V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext} = Open, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	2.85	3.65	mA
		I_{DD}(off) 2	R_{ext} = 744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	5.9	7.9	
		I_{DD}(off) 3	R_{ext} = 372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	8.7	10.7	
		I_{DD}(off) 4	R_{ext} = 186 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	14.4	16.4	
	"ON"	I_{DD}(on) 1	R_{ext} = 744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = On		-	5.8	7.8	
		I_{DD}(on) 2	R_{ext} = 372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = On		-	8.7	10.7	
		I_{DD}(on) 3	R_{ext} = 186 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = On		-	13.5	15.5	

Electrical Characteristics (V_{DD}= 3.3V)

Characteristic		Symbol	Condition		Min.	Typ.	Max.	Unit
Supply Voltage		V_{DD}	-		3.0	3.3	3.6	V
Output Voltage		V_{DS}	$\overline{OUT0}$ ~ $\overline{OUT7}$		-	-	17.0	V
Output Current		I_{OUT}	Test Circuit for Electrical Characteristics		5	-	120	mA
		I_{OH}	SDO		-	-	-1.0	mA
		I_{OL}	SDO		-	-	1.0	mA
Input Voltage	"H" level	V_{IH}	Ta = -40~85ºC		$0.7V_{DD}$	-	V_{DD}	V
	"L" level	V_{IL}	Ta = -40~85ºC		GND	-	$0.3V_{DD}$	V
Output Leakage Current			V_{OH} = 17.0V and channel off		-	-	0.5	μA
Output Voltage	SDO	V_{OL}	I_{OL} = +1.0mA		-	-	0.4	V
		V_{OH}	I_{OH} = -1.0mA		2.9	-	-	V
Output Current 1		I_{OUT1}	V_{DS} = 0.5V	R_{ext} = 744 Ω	-	20.1	-	mA
Current Skew (between channels)		dI_{OUT1}	I_{OUT} = 20.1mA $V_{DS} \geq$ 0.5V	R_{ext} = 744 Ω	-	±1	±3	%
Output Current 2		I_{OUT2}	V_{DS} = 0.6V	R_{ext} = 372 Ω	-	50	-	mA
Current Skew (between channels)		dI_{OUT2}	I_{OUT} = 50mA $V_{DS} \geq$ 0.6V	R_{ext} = 372 Ω	-	±1	±3	%
Output Current vs. Output Voltage Regulation		$\%/dV_{DS}$	V_{DS} within 1.0V and 3.0V		-	±0.1	-	% / V
Output Current vs. Supply Voltage Regulation		$\%/dV_{DD}$	V_{DD} within 3.2V and 3.6V		-	±1	-	% / V
Pull-up Resistor		R_{IN}(up)	$\overline{OE}$		250	500	800	KΩ
Pull-down Resistor		R_{IN}(down)	LE		250	500	800	KΩ
Supply Current	"OFF"	I_{DD}(off) 1	R_{ext} = Open, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	0.78	1.58	mA
		I_{DD}(off) 2	R_{ext} = 744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	3.6	4.4	
		I_{DD}(off) 3	R_{ext} = 372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = Off		-	6.5	7.3	
	"ON"	I_{DD}(on) 1	R_{ext} = 744 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = On		-	3.6	4.2	
		I_{DD}(on) 2	R_{ext} = 372 Ω, $\overline{OUT0}$ ~ $\overline{OUT7}$ = On		-	6.4	7.2	

Test Circuit for Electrical Characteristics



Switching Characteristics (V_{DD}= 5.0V)

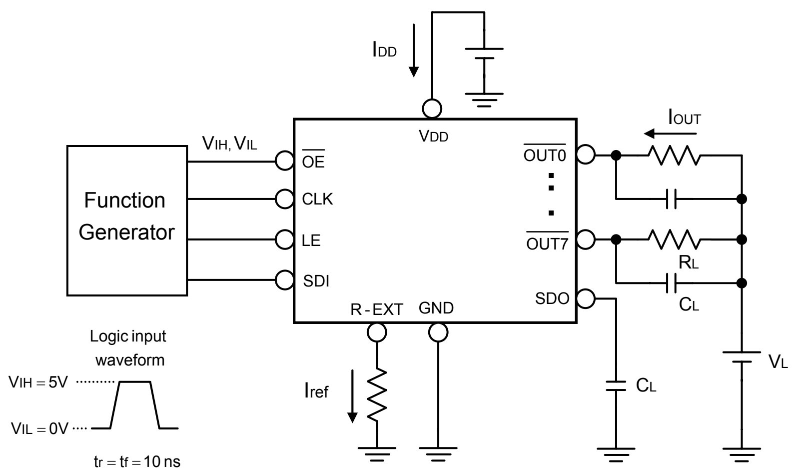
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time (“L” to “H”)	CLK - $\overline{OUTn}$	t_{pLH1}	Test Circuit for Switching Characteristics	-	100	150	ns
	LE - $\overline{OUTn}$	t_{pLH2}		-	100	150	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pLH3}		-	100	150	ns
	CLK - SDO	t_{pLH}		20	25	30	ns
Propagation Delay Time (“H” to “L”)	CLK - $\overline{OUTn}$	t_{pHL1}		-	100	150	ns
	LE - $\overline{OUTn}$	t_{pHL2}		-	100	150	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pHL3}		-	100	150	ns
	CLK - SDO	t_{pHL}		20	25	30	ns
Pulse Width	CLK	$t_{w(CLK)}$	V_{DD} = 5.0 V V_{DS} = 0.8 V V_{IH} = V_{DD} V_{IL} = GND R_{ext} = 372 Ω V_L = 4.0 V R_L = 64 Ω C_L = 10 pF	20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ (@I_{OUT} < 60mA)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		10	-	-	ns
Setup Time for SDI		$t_{su(D)}$		5	-	-	ns
Maximum CLK Rise Time		t_r*		-	-	500	ns
Maximum CLK Fall Time		t_f*		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	120	150	ns
Output Fall Time of Vout (turn on)		t_{of}		-	200	250	ns
Clock Frequency		F_{CLK}	Cascade Operation	-	-	25.0	MHz

*If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

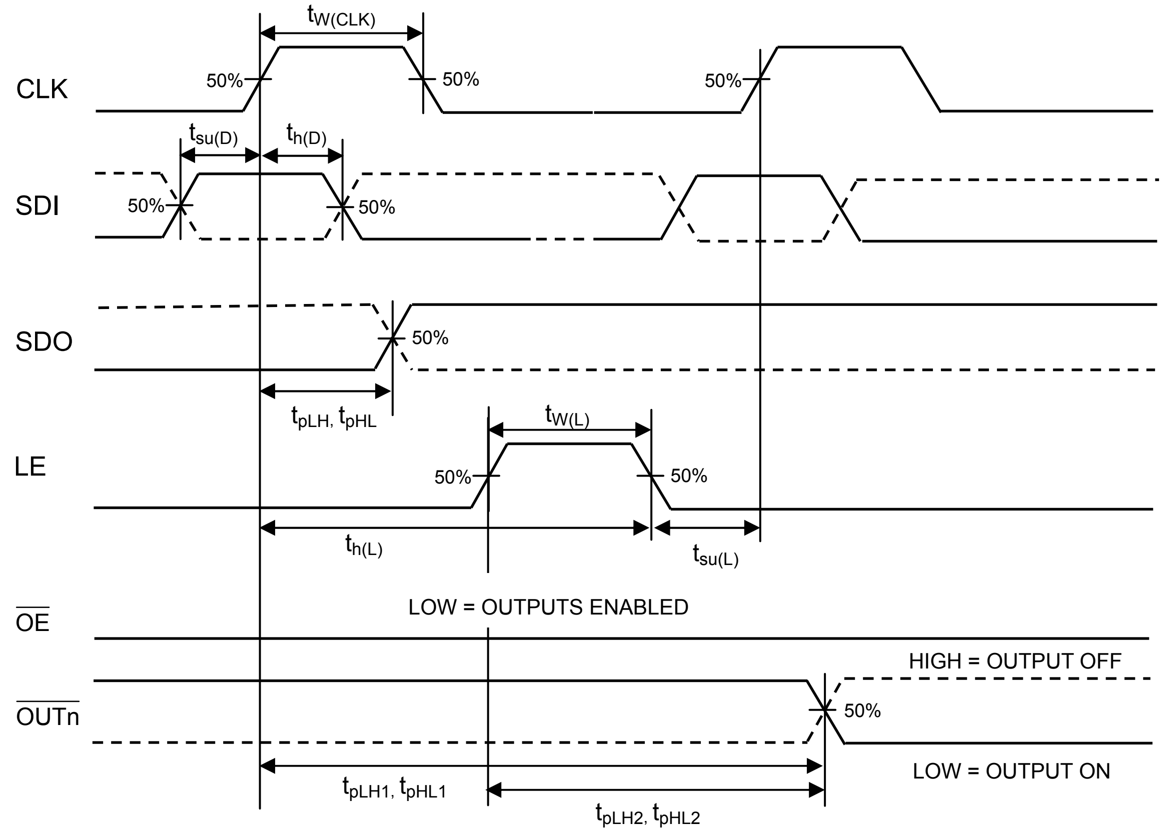
Switching Characteristics (V_{DD}= 3.3V)

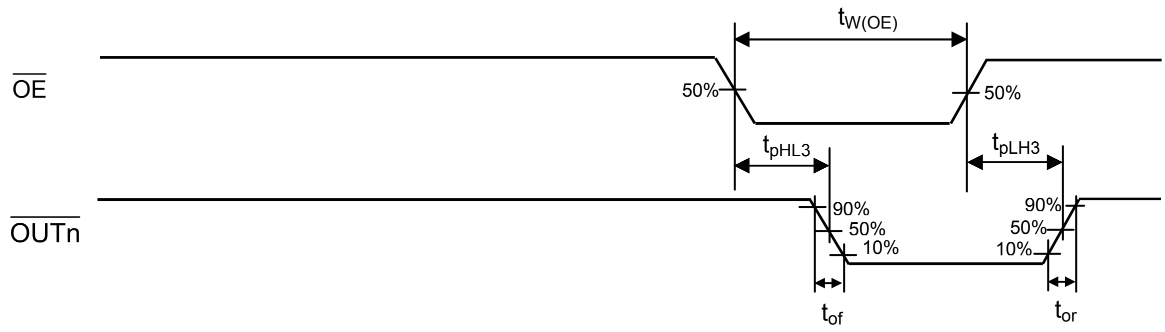
Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK - $\overline{OUTn}$	t_{pLH1}	Test Circuit for Switching Characteristics V_{DD} = 3.3 V V_{DS} = 0.8 V V_{IH} = V_{DD} V_{IL} = GND R_{ext} = 380 Ω V_L = 4.0 V R_L = 64 Ω C_L = 10 pF	-	100	150	ns
	LE - $\overline{OUTn}$	t_{pLH2}		-	100	150	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pLH3}		-	100	150	ns
	CLK - SDO	t_{pLH}		45	55	65	ns
Propagation Delay Time ("H" to "L")	CLK - $\overline{OUTn}$	t_{pHL1}		-	130	200	ns
	LE - $\overline{OUTn}$	t_{pHL2}		-	130	200	ns
	$\overline{OE}$ - $\overline{OUTn}$	t_{pHL3}		-	130	200	ns
	CLK - SDO	t_{pHL}		45	55	65	ns
Pulse Width	CLK	$t_{w(CLK)}$		20	-	-	ns
	LE	$t_{w(L)}$		20	-	-	ns
	$\overline{OE}$ (@I_{OUT} < 50mA)	$t_{w(OE)}$		200	-	-	ns
Hold Time for LE		$t_{h(L)}$		10	-	-	ns
Setup Time for LE		$t_{su(L)}$		5	-	-	ns
Hold Time for SDI		$t_{h(D)}$		10	-	-	ns
Setup Time for SDI		$t_{su(D)}$		5	-	-	ns
Maximum CLK Rise Time		t_r		-	-	500	ns
Maximum CLK Fall Time		t_f		-	-	500	ns
Output Rise Time of Vout (turn off)		t_{or}		-	120	150	ns
Output Fall Time of Vout (turn on)		t_{of}		-	200	400	ns
Clock Frequency		F_{CLK}	Cascade Operation	-	-	12.0	MHz

Test Circuit for Switching Characteristics



Timing Waveform



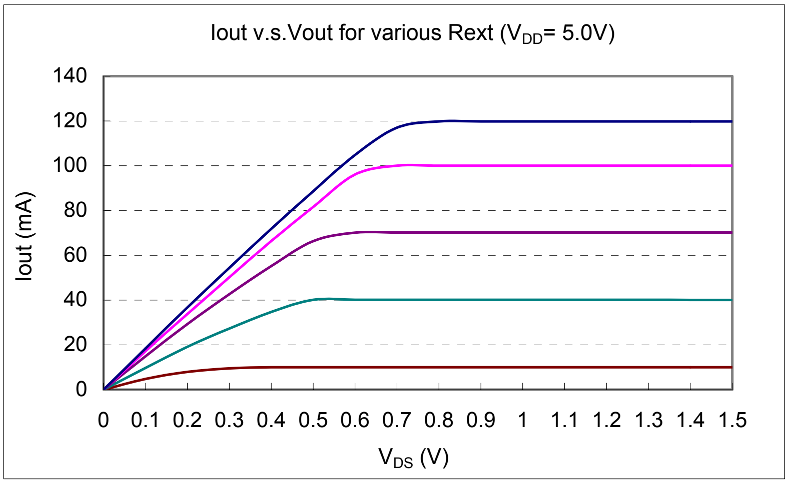


Application Information

Constant Current

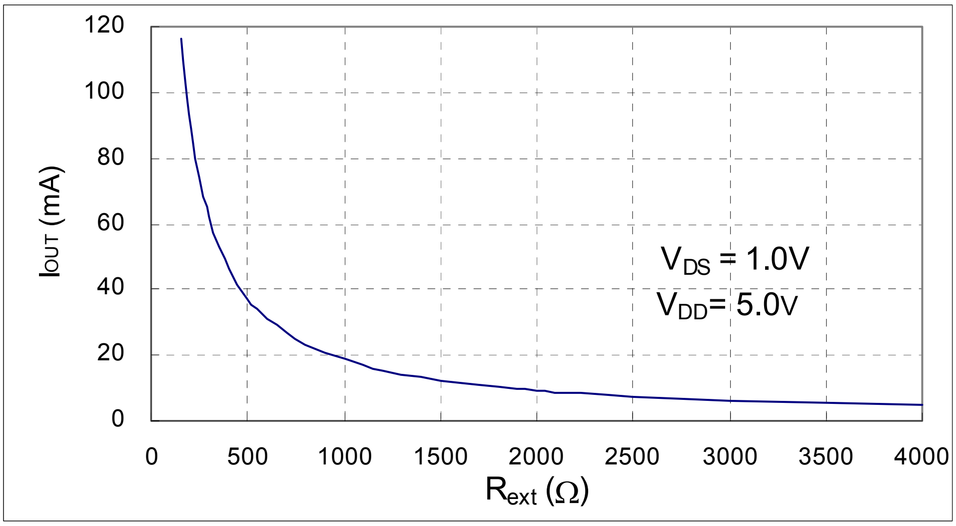
In LED display application, MBI5168 provides nearly no variations in current from channel to channel and from IC to IC. This can be achieved by:

1) While $I_{OUT} \leqq$ 100mA, the maximum current variation between channels is less than ±3%, and that between ICs is less than ±6%.
2) In addition, the characteristics curve of output stage in the saturation region is flat and users can refer to the figure as shown below. Thus, the output current can be kept constant regardless of the variations of LED forward voltages (V_F).



Adjusting Output Current

The output current of each channel (I_{OUT}) is set by an external resistor, R_{ext}. The relationship between I_{OUT} and R_{ext} is shown in the following figure.



Resistance of the external resistor, R_{ext}, in Ω

Also, the output current can be calculated from the equation:

$V_{R\text{-}EXT}$ = 1.253Volt

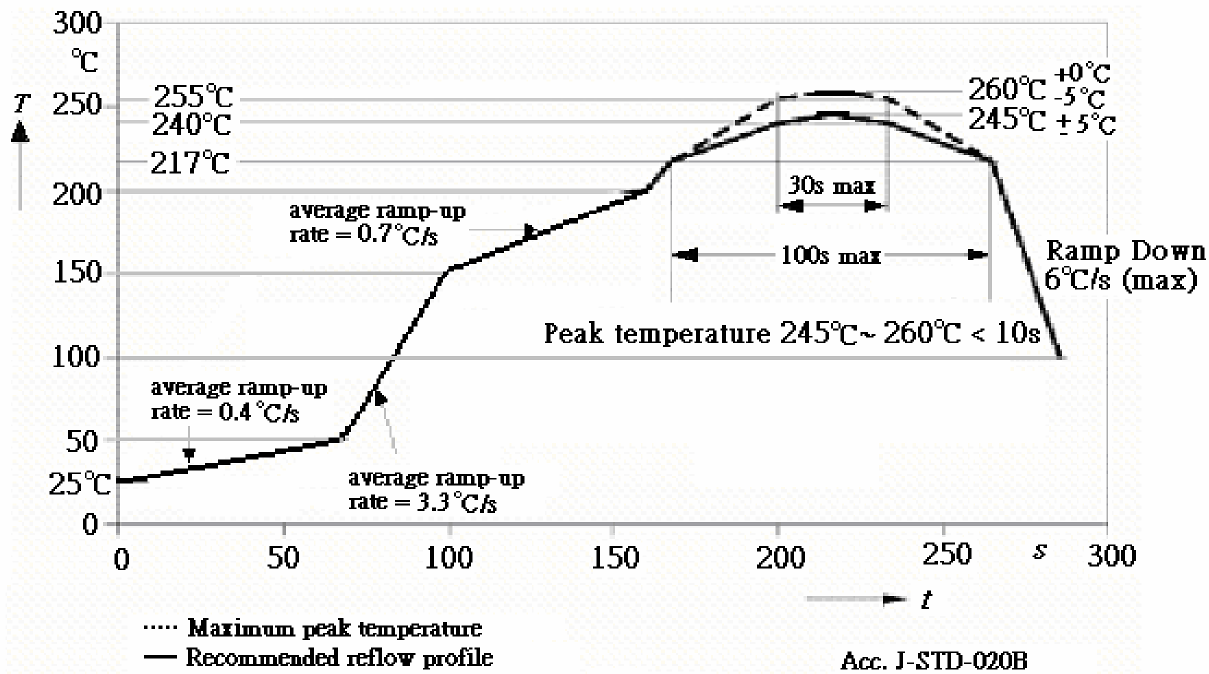
$I_{ref} = V_{rext} / R_{ext}$ if another end of the external resistor R_{ext} is connected to ground.

$I_{OUT} = I_{ref} \times 15$ = 1.253Volt / R_{ext} x 15.

where R_{ext} is the resistance of the external resistor connected to R-EXT terminal and $V_{R\text{-}EXT}$ is the voltage of R-EXT terminal. The magnitude of current (as a function of R_{ext}) is around 50.52mA at 372Ω and 25.26mA at 744Ω (V_{DD}= 5V).

Soldering Process of “Pb-free & Green” Package Plating*

Macroblock has defines "Pb-Free & Green" to mean semiconductor products that are compatible with the current RoHS requirements and selected **100% pure tin** (Sn) to provide forward and backward compatibility with both the current industry-standard SnPb-based soldering processes and higher-temperature Pb-free processes. Pure tin is widely accepted by customers and suppliers of electronic devices in Europe, Asia and the US as the lead-free surface finish of choice to replace tin-lead. Also, it is backward compatible to standard 215ºC to 240ºC reflow processes which adopt tin/lead (SnPb) solder paste. However, in the whole Pb-free soldering processes and materials, 100% pure tin (Sn), will all require up to 260°C for proper soldering on boards, referring to J-STD-020B as shown below.



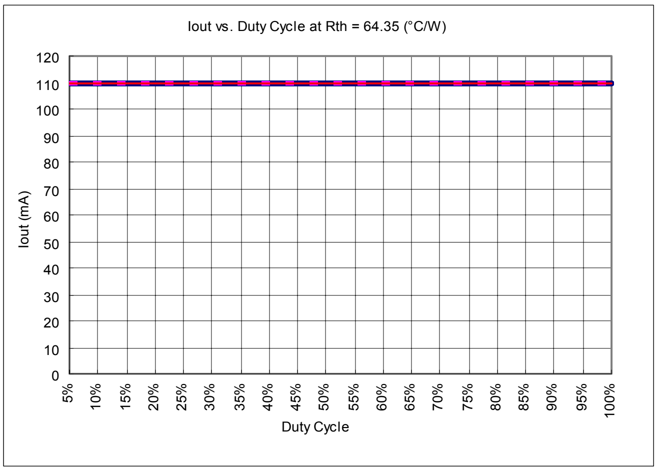
*Note1: For details, please refer to Macroblock’s “Policy on Pb-free & Green Package”.

Package Power Dissipation (P_D)

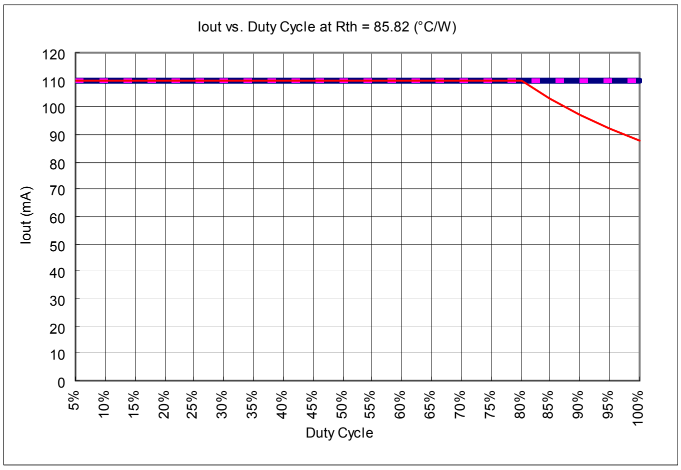
The maximum allowable package power dissipation is determined as $P_D(max) = (Tj – Ta) / R_{th(j-a)}$. When 8 output channels are turned on simultaneously, the actual package power dissipation is $P_D(act) = (I_{DD} \times V_{DD}) + (I_{OUT} \times Duty \times V_{DS} \times 8)$. Therefore, to keep $P_D(act) \le P_D(max)$, the allowable maximum output current as a function of duty cycle is:

$I_{OUT} = \{ [(Tj – Ta) / R_{th(j-a)}] – (I_{DD} \times V_{DD}) \} / V_{DS} / Duty / 8$,

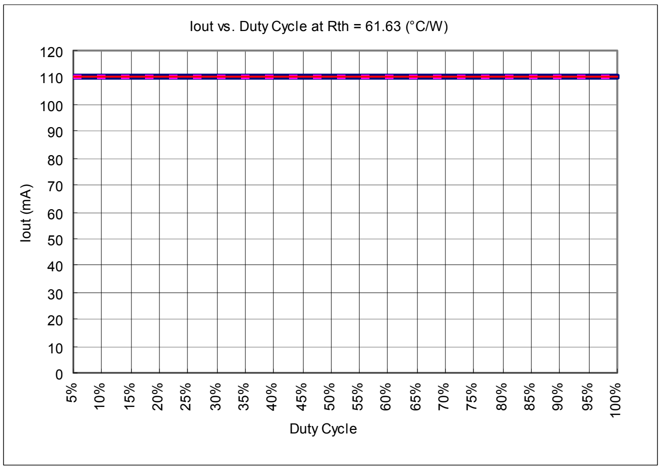
where Tj = 150°C.



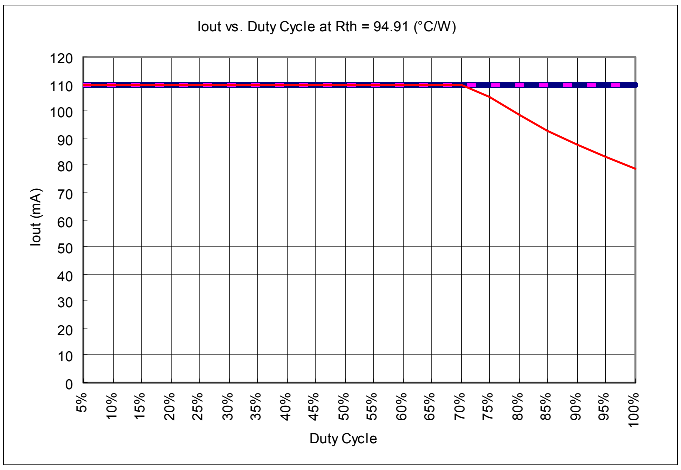
CN\GN Device Type



CD\GD Device Type



CDW\GDW Device

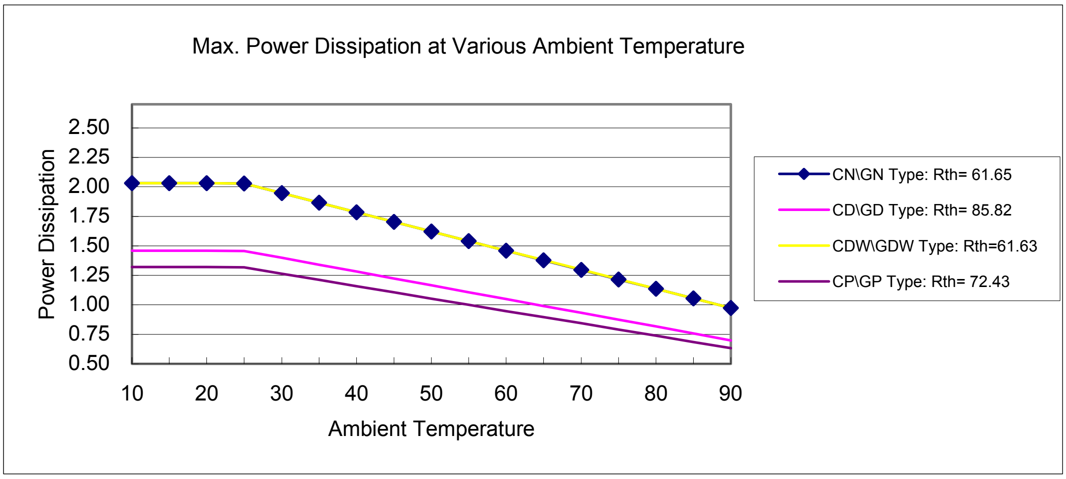


CP\GP Device Type

Condition：V_{DS} = 1.0V, V_{DD}= 5.0V, 8 output channels active，Ta is listed in the below legends.

Device Type		$R_{th(j-a)}$(°C/W)		Note
CN	GN	64.35	60.20	25℃ (solid blue), 55℃ (dashed pink), 85℃ (solid red)
CD	GD	85.82	70.14	
CDW	GDW	61.63	68.67	
CP	GP	94.91	80.00	

The maximum power dissipation, $P_D(max) = (Tj - Ta) / R_{th(j-a)}$, decreases as the ambient temperature increases.

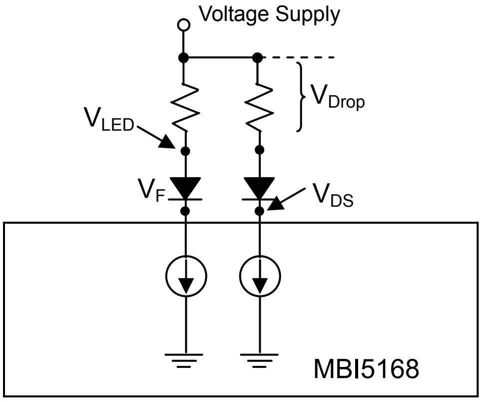


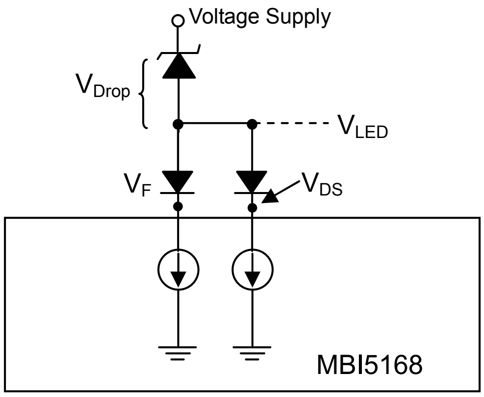
Load Supply Voltage (V_{LED})

MBI5168 are designed to operate with V_{DS} ranging from 0.4V to 1.0V considering the package power dissipating limits. V_{DS} may be so high as to make $P_{D(act)} > P_{D(max)}$ under higher V_{LED}, for instance, than 5V, where $V_{DS} = V_{LED} - V_F$ and V_{LED} is the load supply voltage. In this case, it is recommended to use the lowest possible supply voltage or to set an external voltage reducer, V_{DROP}.

A voltage reducer lets $V_{DS} = (V_{LED} - V_F) - V_{DROP}$.

Resistors or Zener diode can be used in the applications as shown in the following figures.

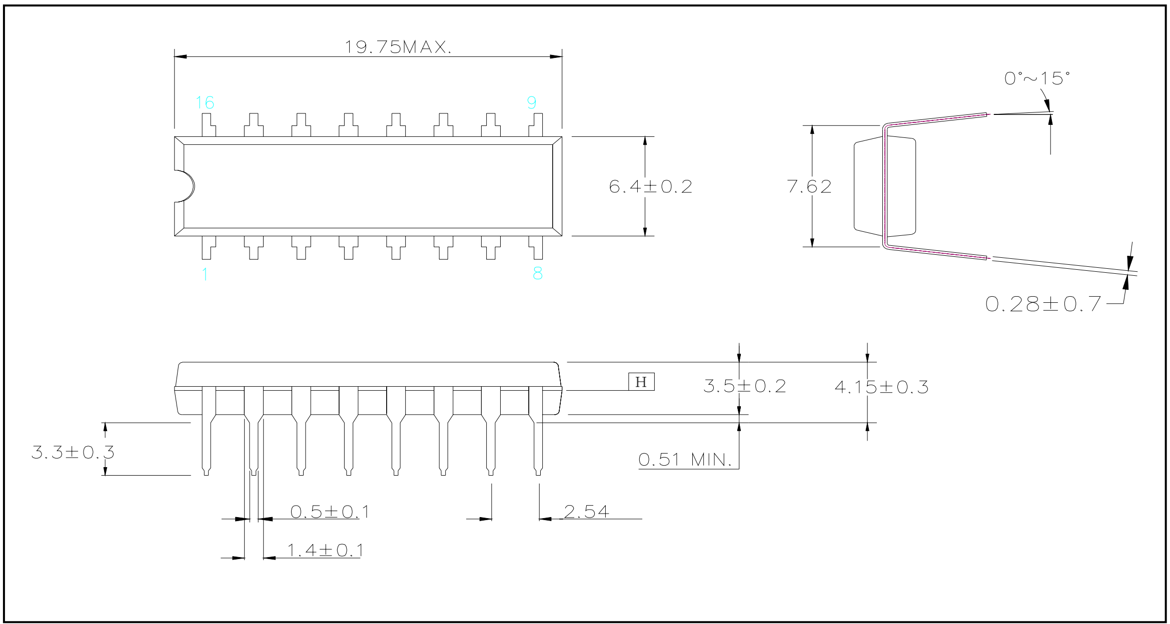




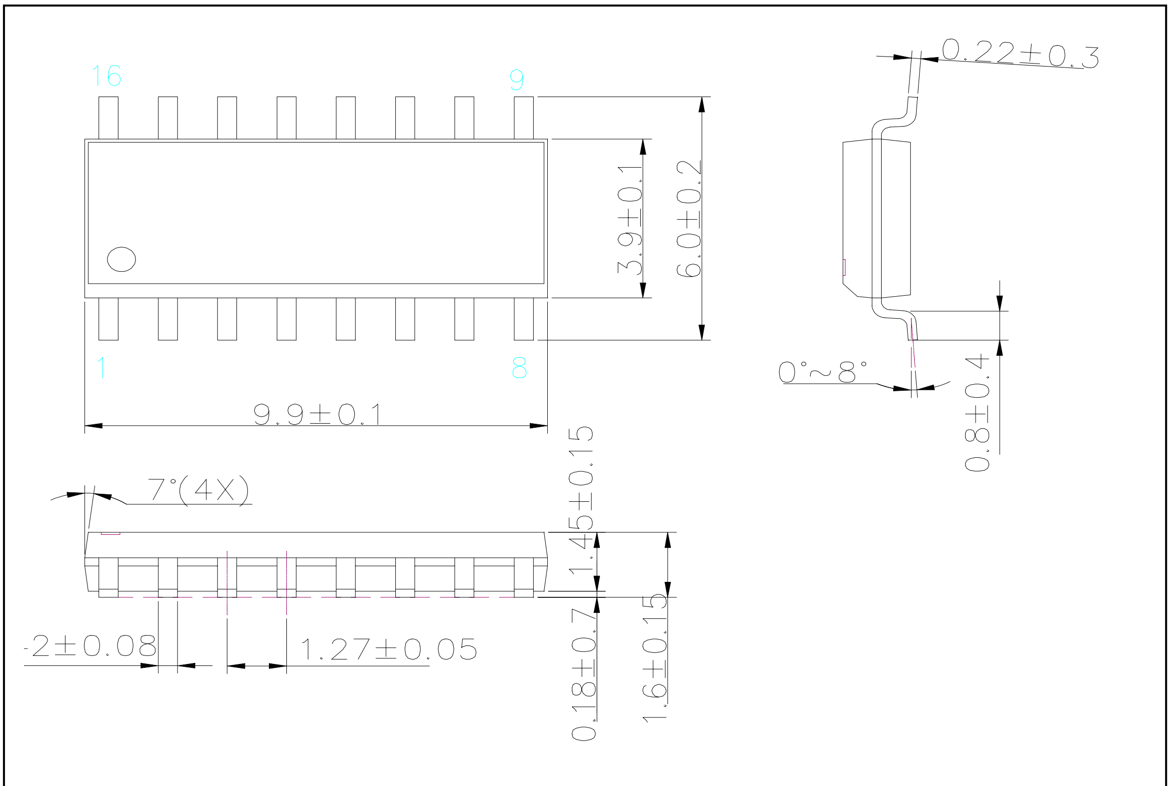
Switching Noise Reduction

LED Driver ICs are frequently used in switch-mode applications which always behave with switching noise due to parasitic inductance on PCB. To eliminate switching noise, refer to "Application Note for 8-bit and 16-bit LED Drivers- Overshoot".

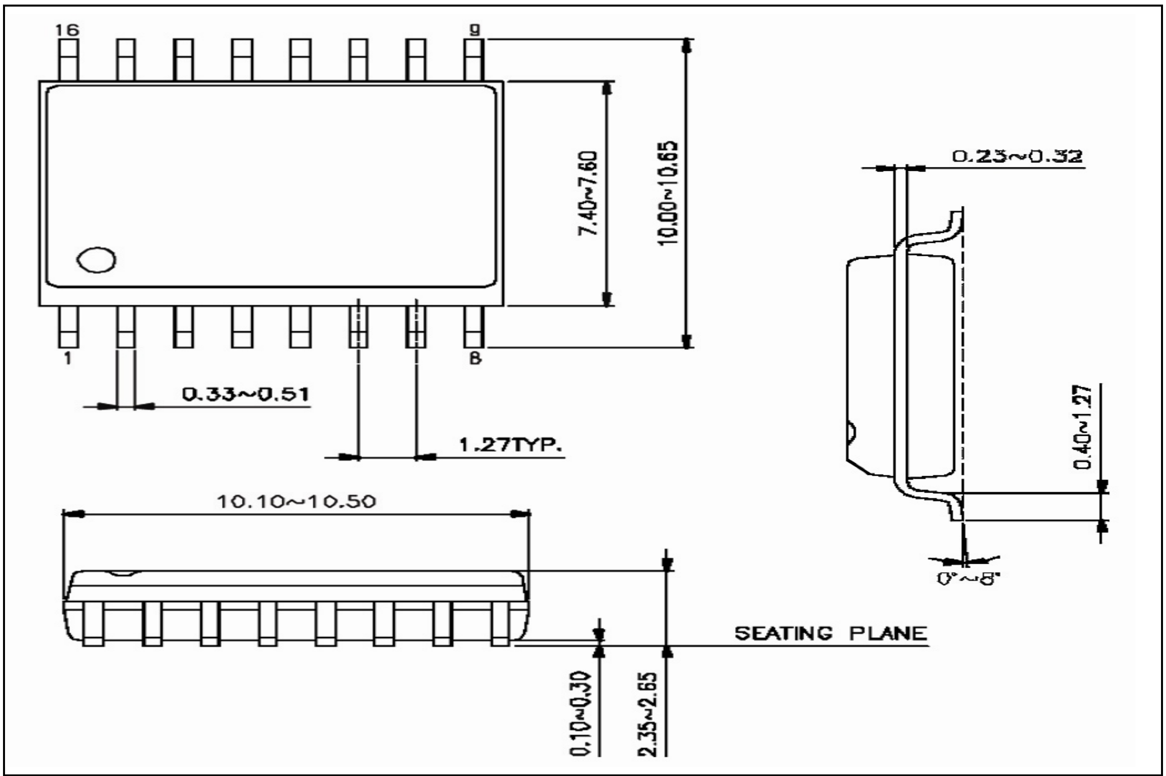
Outline Drawings



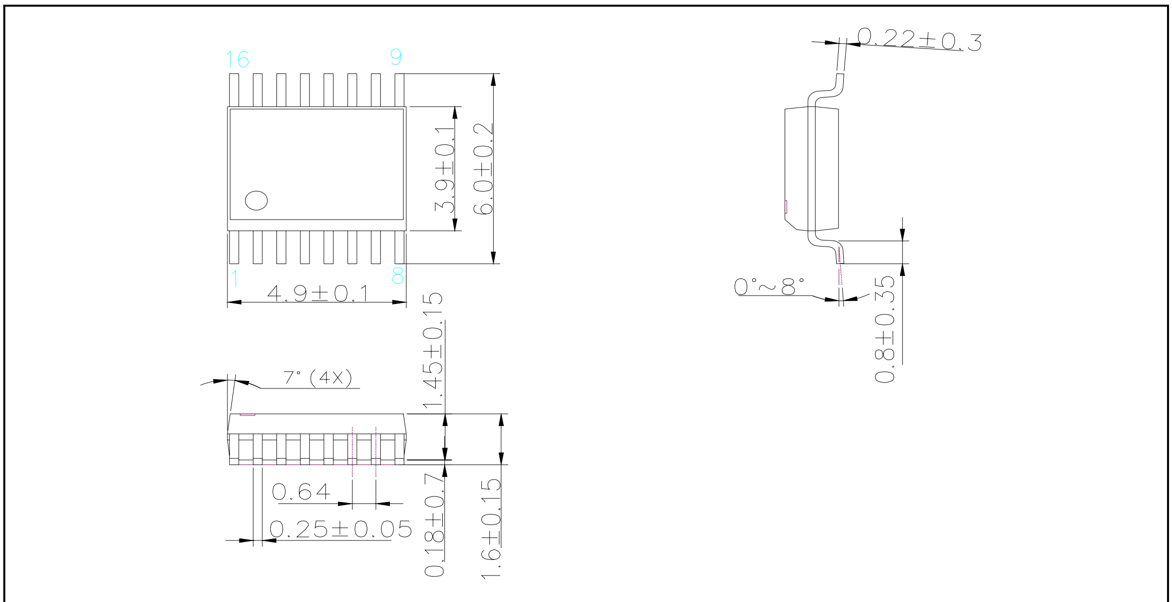
MBI5168CN\GN Outline Drawing



MBI5168CD\GD Outline Drawing



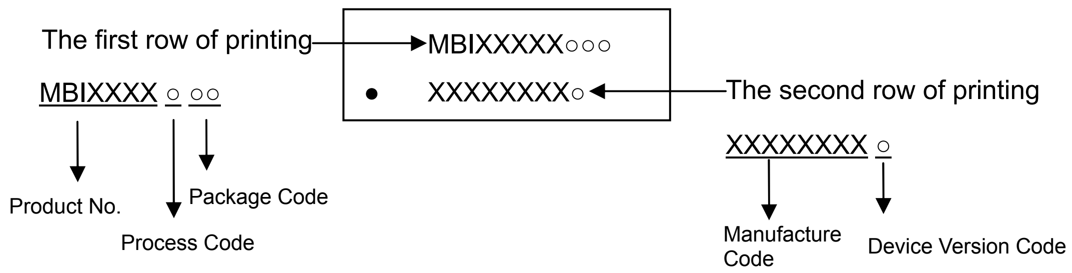
MBI5168CDW\GDW Outline Drawing



MBI5168CP\GP Outline Drawing

Note: The unit for the outline drawing is mm.

Product Top-mark Information



Product Revision History

Datasheet version	Device version code
VA.00	*Not defined*
VA.02	A

Product Ordering Information

Part Number	Package Type	Weight (g)
MBI5168CN	P-DIP16-300-2.54	1.02
MBI5168CD	SOP16-150-1.27	0.13
MBI5168CDW	SOP16-300-1.27	0.37
MBI5168CP	SSOP16-150-0.64	0.07

Part Number	"Pb-free & Green" Package Type	Weight (g)
MBI5168GN	P-DIP16-300-2.54	1.02
MBI5168GD	SOP16-150-1.27	0.13
MBI5168GDW	SOP16-300-1.27	0.37
MBI5168GP	SSOP16-150-0.64	0.07